REMARKS

Applicants submit that claims 7-12, 18-24 have been canceled hereby, and claims 13-17, 25-33 are remained unchanged, while no new matter entered.

Claim Rejections-35 USC §102

The Office Action rejected claims 7-33 under 35 U.S.C. 102(b) as being anticipated by Rajeevakumar US Patent 5,426,324.

In response to the rejection to claims 7-33 under 35 U.S.C. 102(b) as being anticipated by Rajeevakumar US Patent 5,426,324, Applicants have canceled claims 7-12, 18-24, and hereby otherwise traverse this rejections. As such, Applicant submits that claims 13-17, 25-33 are now in condition for allowance.

With respect to claim 13, as originally filed, recites in part:

A trench capacitor, comprising:

> ... a second capacitor dielectric layer between said protruding electrode and said substrate, said substrate around said first and second capacitor dielectric layers being a bottom electrode; and
> a conducting structure electrically connecting said protruding electrode and said conducting layer, wherein said conducting layer, said protruding electrode, and said conducting structure serve as an upper electrode.

Applicant submits that such a trench capacitor, as set forth in claim 13 is neither taught, disclosed, nor suggested by Rajeevakumar '324 or any of the other cited references, taken alone or in combination.

Rajeevakumar '324 fails to disclose, teach or suggest a "**second capacitor dielectric layer**" which is required for the trench capacitor as set forth in claim 13 (Emphasis added.). Therefore, claim 13 as previously presented should not be considered as being anticipated by Rajeevakumar '324 or any of the other cited references, taken alone or in combination.

The Examiner alleged that Rajeevakumar '324 teaches a second capacitor layer (gate oxide layer) 4a (FIG. 8). However, the gate oxide layer 4a is presented in FIGS. 7 and 8 only. FIGS. 3-7, 8, 8a and 9-13 show the sequential process steps for fabricating an SRAM cell in accordance with the present invention (Column 2, lines 15-17). It is believed that only those matters presented in FIGS. 1 and 2 are elements of the final product (a trench capacitor or an SRAM cell) of Rajeevakumar '324, which can be taken for comparison with the present invention. Therefore, any element, i.e., the gate oxide layer 4a, presented during the fabricating process, but cannot be found in the final product should not be used as evidence of any anticipation. It is clearly shown in FIG. 1, that the gate poly 2 is directly configured on the trench poly node 11. Therefore, there is no **second capacitor layer** "between said protruding electrode and said substrate" disclosed in accordance with Rajeevakumar '324 (Emphasis added.).

Accordingly, the present invention as set forth in claim 13 should not be considered as being anticipated by Rajeevakumar '324, and claim 13 should be allowable.

If independent claim 13 is allowable over the prior art of record, then its dependent claims 13-17 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

With respect to claim 25, as originally filed, recites in part:

> A dynamic random access memory cell, the memory cell comprising:
> > ... a second capacitor dielectric layer between said protruding electrode and said substrate, said substrate around said first and second capacitor dielectric layers being a bottom electrode;
> > ...
> > a gate dielectric layer between said gate electrode and said substrate; and
> > a conducting structure electrically connecting said protruding electrode and said conducting layer, and said conducting layer, said protruding electrode, and said conducting structure being an upper electrode

Applicant submits that such a dynamic random access memory cell, as set forth in claim 25 is neither taught, disclosed, nor suggested by Rajeevakumar '324 or any of the other cited references, taken alone or in combination.

For the similar reason as discussed above, Rajeevakumar '324 fails to teach, disclose or suggest a **"second capacitor dielectric layer"** which is required for the dynamic random access memory cell, as set forth in claim 25. Further, without such a second capacitor dielectric layer, the bottom electrode as set forth in claim 25 is also not taught, disclosed or suggested by Rajeevakumar '324. Furthermore, Rajeevakumar '324 teaches a $TiSi_2$ layer 14, which is well

known as a good electric conductor, disposed between the multilevel contact 8 (alleged as a conducting structure), the trench poly node 11 (alleged as a conducting layer), the gate poly 2 (alleged as a protruding electrode) are electrically connected with the diffusion 13 (alleged as drain/source regions) (FIG. 1; Column 2, lines 34 and 43-45). That means that all elements alleged for composing an upper electrode are electrically connected with the drain/source regions 13. However, it is well known to those with ordinary skills in the art that the electrode electrically connected with a source/drain is a lower electrode, rather than an upper electrode. In other words, Rajeevakumar '324 doesn't teach, disclose or suggest an upper electrode, and/or a lower electrode as set forth in claim 25.

Accordingly, the present invention as set forth in claim 25 should not be considered as being anticipated by Rajeevakumar '324, and claim 25 should be allowable.

If independent claim 25 is allowable over the prior art of record, then its dependent claims 26-33 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 13-17, 25-33 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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Date: 12/30/2005

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